FIG.1

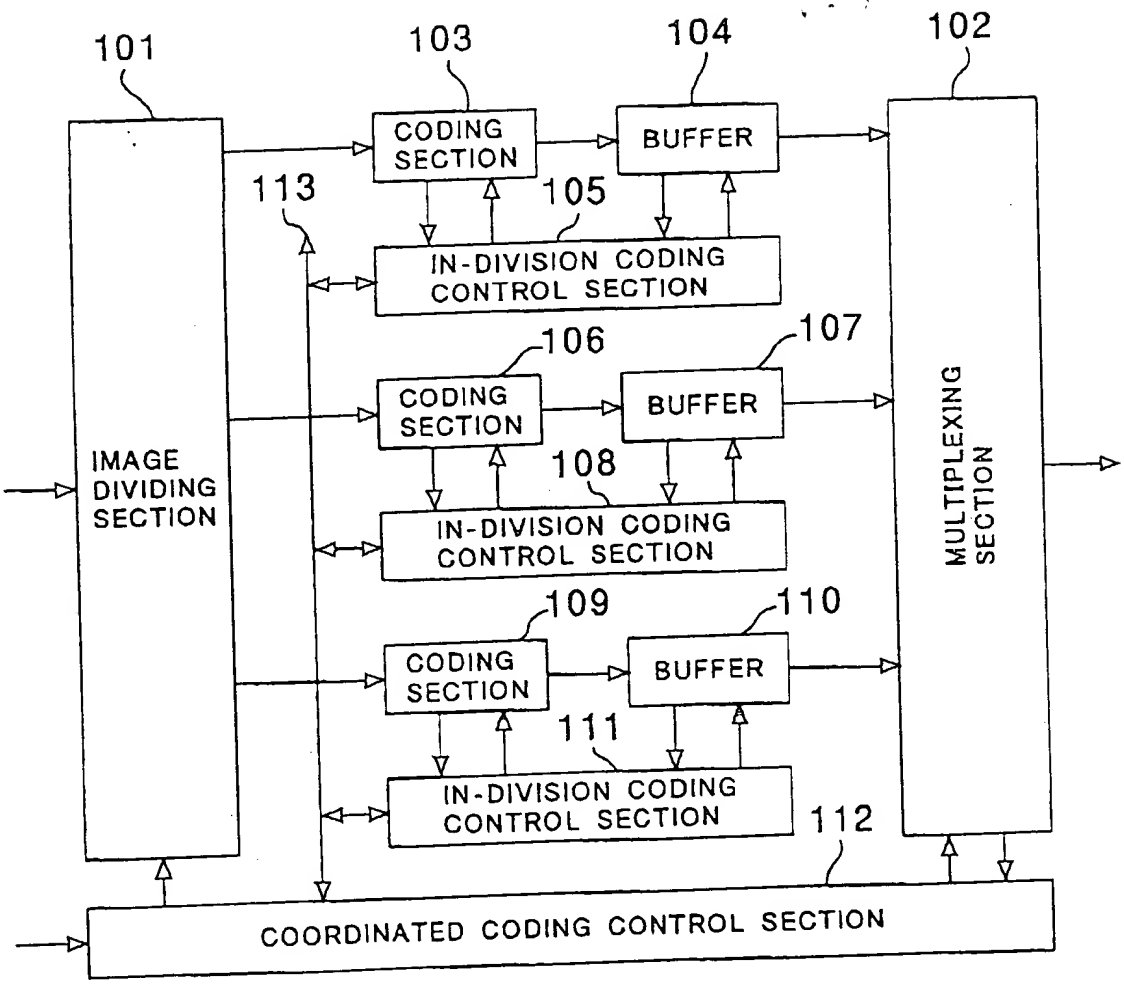

101
103
104
102
CODING SECTION
BUFFER
113
105
IN-DIVISION CODING CONTROL SECTION
106
107
CODING SECTION
BUFFER
IMAGE DIVIDING SECTION
108
IN-DIVISION CODING CONTROL SECTION
MULTIPLEXING SECTION
109
110
CODING SECTION
BUFFER
111
IN-DIVISION CODING CONTROL SECTION
112
COORDINATED CODING CONTROL SECTION

FIG.2(A)

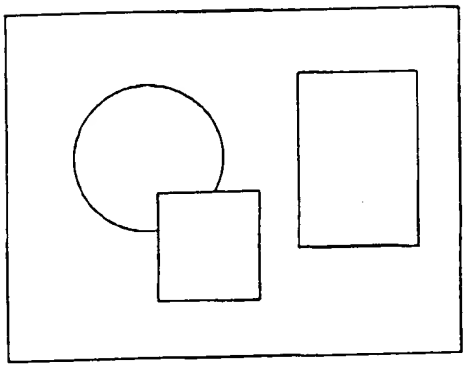


FIG.2(B)

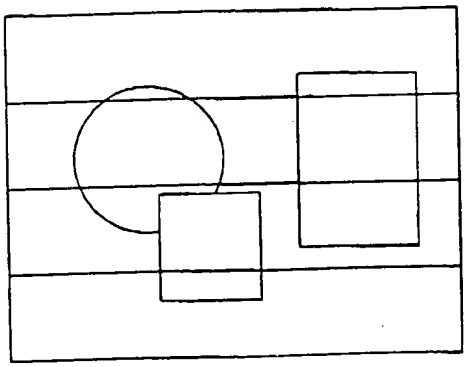


FIG.2(C)

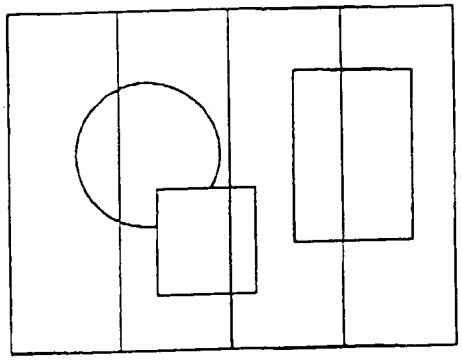


FIG.2(D)

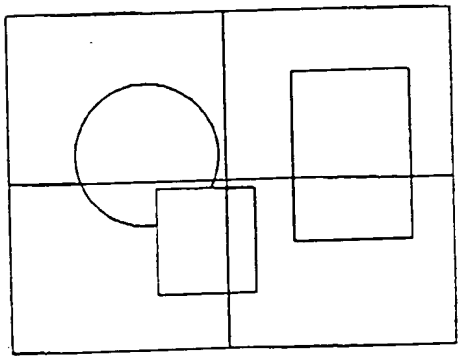


FIG.3(A)

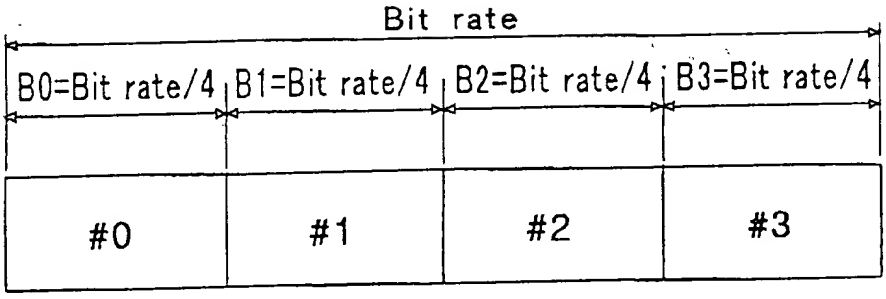

Bit rate
B0=Bit rate/4
B1=Bit rate/4
B2=Bit rate/4
B3=Bit rate/4
#0
#1
#2
#3

FIG.3(B)

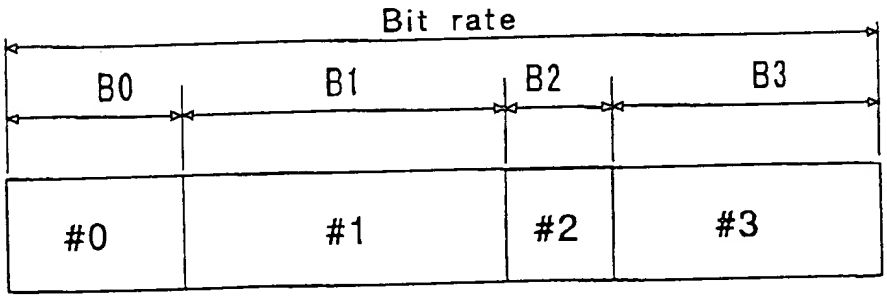

Bit rate
B0
B1
B2
B3
#0
#1
#2
#3

FIG.4

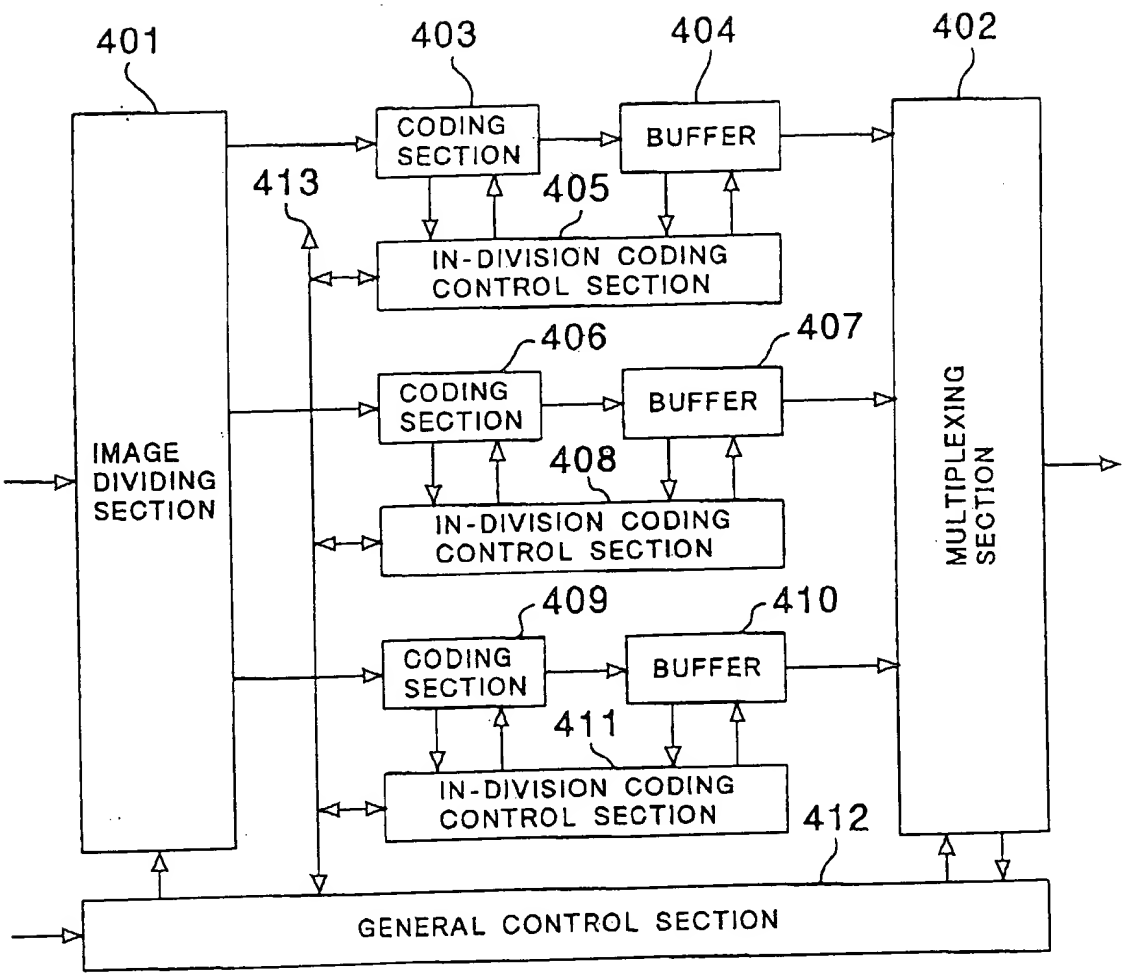
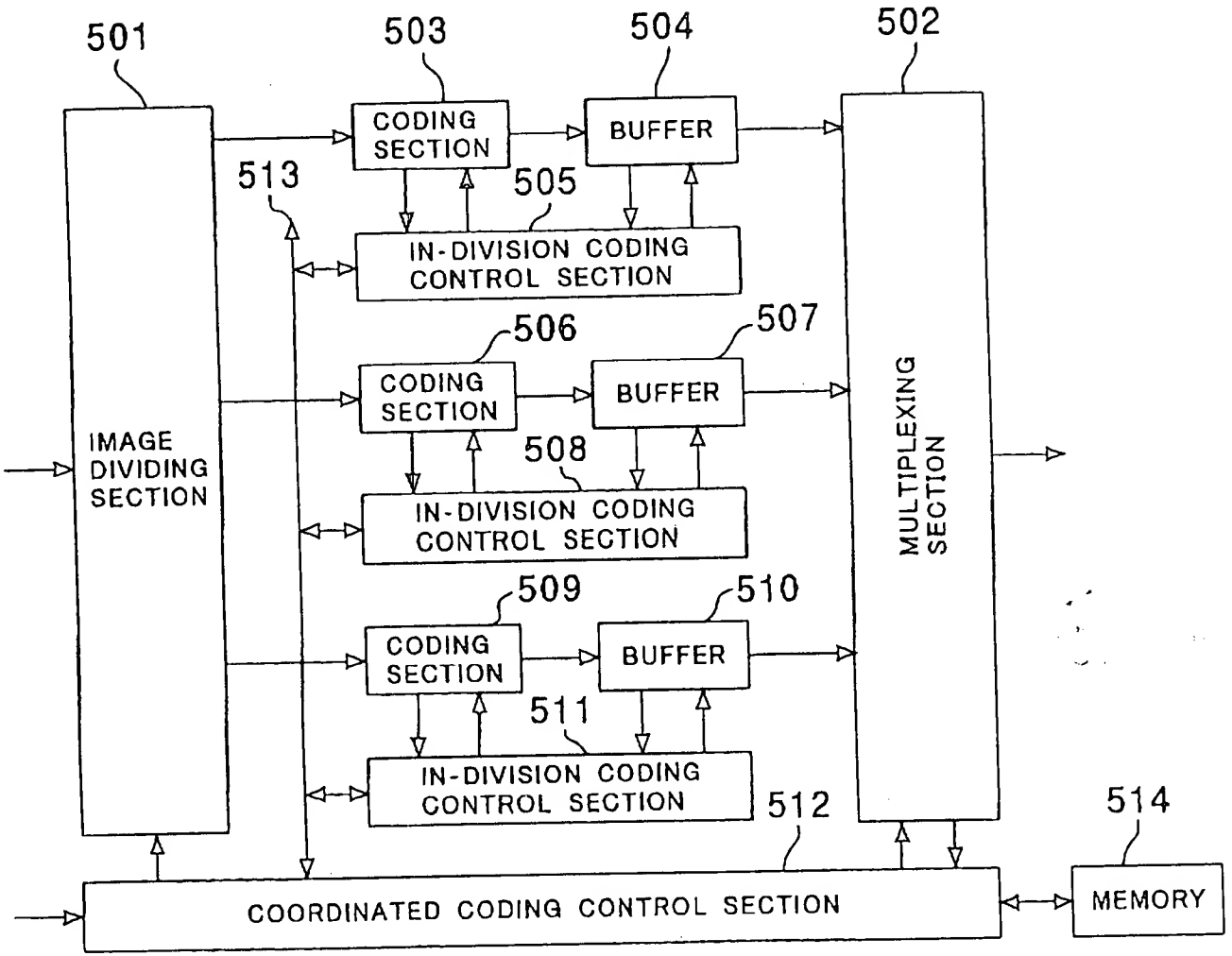

401
403
404
402
CODING SECTION
BUFFER
413
405
IN-DIVISION CODING CONTROL SECTION
406
407
CODING SECTION
BUFFER
IMAGE DIVIDING SECTION
408
IN-DIVISION CODING CONTROL SECTION
MULTIPLEXING SECTION
409
410
CODING SECTION
BUFFER
411
IN-DIVISION CODING CONTROL SECTION
412
GENERAL CONTROL SECTION

FIG.5


501
503
504
502
CODING SECTION
BUFFER
513
505
IN-DIVISION CODING CONTROL SECTION
506
507
CODING SECTION
BUFFER
IMAGE DIVIDING SECTION
508
IN-DIVISION CODING CONTROL SECTION
MULTIPLEXING SECTION
509
510
CODING SECTION
BUFFER
511
IN-DIVISION CODING CONTROL SECTION
512
514
COORDINATED CODING CONTROL SECTION
MEMORY